

ABSTRACTCARRY SAVE ADDERS

A carry save adder circuit for reducing the number of inputs to a lower number of outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third and fourth carry save adders being arranged to provide said outputs, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs.

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